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PATENT

Attorney Docket No.: 000939-052180US

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By: 

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Harold S. Crafts

Application No.: Not Yet Assigned

Filed:

For: SEA-OF-CELLS ARRAY OF
TRANSISTORS

Examiner:

Art Unit:

INFORMATION DISCLOSURE
STATEMENT UNDER 37 CFR §1.97 and
§1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

Applicants also wish to make the Examiner aware of the following co-pending patent applications:

U.S. Patent Application No. 10/125,925
Inventor: Crafts, H.S.
Filing Date: April 19, 2002

U.S. Patent Application No. 10/463,160
Inventor: Crafts, H.S.
Filing Date: June 16, 2003

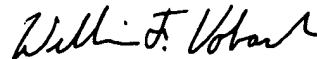
U.S. Patent Application No. 10/601,351
Inventor: Crafts, H.S.
Filing Date: June 23, 2003

To comply with 37 CFR §1.98(a)(2)(iii), enclosed are the specifications, claims and drawings for the above applications.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



William F. Vobach
Reg. No. 39,411

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(use as many sheets as necessary)*

Sheet 2 of 3

Complete if Known

Application Number	Not Yet Assigned
Filing Date	
First Named Inventor	Crafts, Harold S.
Art Unit	
Examiner Name	
Attorney Docket Number	000939-052180US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	A1	US-3,461,361	08/01/1969	Delivorias	
	A2	US-4,143,178	03/06/1979	Harada et al.	
	A3	US-4,151,635	05/01/1979	Kashkooli et al.	
	A4	US-4,229,756	10/21/1980	Sata et al.	
	A5	US-4,244,001	01/06/1981	Alfred C. Ipri	
	A6	US-4,317,690	03/02/1982	Koomen et al.	
	A7	US-4,525,809	06/25/1985	Chiba et al.	
	A8	US-4,584,653	04/22/1986	Chih et al.	
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	A10	US-4,630,219	12/16/1986	DiGiacomo et al.	
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Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT***(use as many sheets as necessary)***Complete if Known**

Application Number	Not Yet Assigned
Filing Date	
First Named Inventor	Crafts, Harold S.
Art Unit	
Examiner Name	
Attorney Docket Number	000939-052180US

Sheet 2 of 3

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	A42	US-5,341,049		08/23/1994	Shimizu et al.	
	A43	US-5,342,794		08/30/1994	Wei, Yi-Hen	
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	A50	US-5,541,120		07/30/1996	Robinson et al.	
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	A52	US-5,671,397		09/23/1997	Crafts	
	A53	US-5,869,900		02/09/1999	Crafts	
	A54	US-6,269,466		07/31/2001	Crafts	
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	A56	US-6,605,499		08/12/2003	Crafts	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
	C1							<input type="checkbox"/>
	C2							<input type="checkbox"/>
	C3							<input type="checkbox"/>

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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		<i>Application Number</i>	Not Yet Assigned
		<i>Filing Date</i>	
		<i>First Named Inventor</i>	Crafts, Harold S.
		<i>Art Unit</i>	
		<i>Examiner Name</i>	
(use as many sheets as necessary)		<i>Attorney Docket Number</i>	000939-052180US
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C1	BACHELU et al. "A Study of the Use of Local Interconnect in CMOS Leaf Cell Design," <i>IEEE</i> , 1993, pp. 566-570	
	C2	BACHELU et al. "A Study of the Use of Local Interconnect in CMOS Leaf Cell Design," <i>IEEE</i> , pp. 1258-1261, 1992	
	C3	BARTELINK et al. "Interconnect for Submicron ASICs," <i>IEEE</i> , 1989, pp. 59-62	
	C4	CHANG, M. & CHEN, C. "PROMPT3 - A cell-Based Transistor Sizing Program Using Heuristic and Simulated Annealing Algorithms." <i>IEEE</i> , 1989, pp. 17.2.1-17.2.4.	
	C5	FELDMAN, J. et al. "An Efficient Algorithm for some Multirow Layout Problems", <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems</i> , August 1993, pp. 1178-1185, Vol. 12, No. 8.	
	C6	HSIEH et al. "Size Optimization for CMOS Basic Cells of VLSI", <i>IEEE</i> , pp. 2180-2183	
	C7	KAWASAKI, H. et al. "10K-Gate GaAs JFET Sea of Gates", <i>IEEE Journal of Solid-State Circuits</i> , October 1991; pp. 1367-1370, Vol. 26, No. 10.	
	C8	KORTE, B. et al. "A Design-System for ASIC's with Macrocells", <i>IEEE, Euro ASIC '90</i> ; 1990; pp. 220-224.	
	C9	KORTE, B. et al. "Combining Partitioning and Global Routing in a Sea-of-Cells Design", <i>IEEE Computer-Aided Design, 1989 International Conference</i> ; pp. 98-101	
	C10	MADIHIAN, M. et al. "Application of AlGaAs/GaAs HBT's to High-Speed CML Logic Family Fabrication", <i>IEEE Transactions on Electron Devices</i> , April 1989; pp. 625-631, Vol. 36, No. 4.	
	C11	PANNER, J. et al. "A Comprehensive CAD System for High-Performance 300K-Circuit ASIC Logic Chips", <i>IEEE Journal of Solid-State Circuits</i> , March 1991, pp. 300-309, Vol. 26, No. 3.	
	C12	PERELLO et al. "Dependence of Spice level 3 Model Parameters with tRansistor Size", <i>IEEE</i> , pp. 84-89.	
	C13	SHICHIJO, H. et al. "GaAs MESFET and Si CMOS Cointegration and Circuit Techniques", <i>IEEE, GaAs IC Symposium</i> , September 1988; pp. 239-242.	
	C14	STOOPS, E.H., Structured Macro, <i>IBM Technical Disclosure Bulletin</i> , September 1982, Vol. 25, No. 4	

Examiner Signature	Date Considered
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